HORIZONTAL MEMORY DEVICES WITH VERTICAL GATES

Abstract of the Disclosure

Structures and methods for memory devices are provided which operate with lower control gate voltages than conventional floating gate transistors, and which do not increase the costs or complexity of the device fabrication process. In one embodiment of the present invention, the novel memory cell includes a source region and a drain region separated by a channel region in a horizontal substrate. A first vertical gate is separated from a first portion of the channel region by a first oxide thickness. A second vertical gate is separated from a second portion of the channel region by a second oxide thickness. According to the teachings of the present invention, the total capacitance of these memory devices is about the same as that for the prior art of comparable source and drain spacings. However, according to the teachings of the present invention, the floating gate capacitance (CFG) is much smaller than the control gate capacitance (CCG) such that the majority of any voltage applied to the control gate will appear across the floating gate thin tunnel oxide.